IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A reconfigurable input/output controller (IOC) coupled via an interconnection network to a plurality of nodes in an adaptive computing engine (ACE), wherein the coupling includes an interconnection network, the reconfigurable IOC comprising:

at least one input coupled to the interconnection network for receiving a point-to-point transfer instruction for a device internal to the ACE; and

at least one output for providing a translated point-to-point transfer instruction to an external device.

Claims 2-3 (Canceled)

Claim 4 (Withdrawn): A physical link adapter comprising

a first configurable coupling to a first connector, wherein the first connector receives a first set of signals of a first communication type;

a second configurable coupling to a second connector, wherein the second connector receives a second set of signals of a second communication type; and

a controller for selectively applying an output of either the first or second configurable coupling to a common bus.

Claim 5 (Currently Amended): The reconfigurable IOC of claim 1, wherein a translated point-to-point transfer instruction provides translation of a port number [[from]] in the adaptive computing engine to the external device.

Claim 6 (Previously Presented): The reconfigurable IOC of claim 1, wherein a translated point-to-point transfer instruction provides translation of an address from the adaptive computing engine to the external device.

Claim 7 (Previously Presented): The reconfigurable IOC of claim 1, further comprising Peek/Poke service circuitry.

Claim 8 (Previously Presented): The reconfigurable IOC of claim 1, further comprising memory random access circuitry.

Claim 9 (Previously Presented): The reconfigurable IOC of claim 1, further comprising direct memory access circuitry.

Claim 10 (Previously Presented): The reconfigurable IOC of claim 1, further comprising real time input circuitry.

Claim 11 (Previously Presented): The reconfigurable IOC of claim 1, further comprising a status line coupled to the external device for indicating an availability of services.

Claim 12 (Previously Presented): The reconfigurable IOC of claim 1, further comprising a physical link adapter coupled to an input of the configurable IOC.

Claim 13 (Previously Presented): The reconfigurable IOC of claim 12, further comprising; coupling circuitry coupled to the physical link adapter; and
a plurality of different physical connectors coupled to the coupling circuitry.

Claim 14 (Previously Presented): The reconfigurable IOC of claim 13, further comprising:

a reconfigurable finite-state machine for controlling the coupling circuitry to selectively connect a signal from a physical connector.

Claim 15 (Previously Presented): The reconfigurable IOC of claim 1, wherein the interconnection network enables communication among a plurality of nodes and interfaces to reconfigure the ACE for a variety of tasks.

Claim 16 (Previously Presented): The reconfigurable IOC of claim 1, wherein the IOC runs at the interconnect network clock rate.

Claim 17 (Previously Presented): The reconfigurable IOC of claim 1, wherein the external devices include at least one ACE, and at least one system on a chip (SOC).

Claim 18 (Previously Presented): The reconfigurable IOC of claim 17, wherein the IOC includes status lines to the SOC, the SOC being responsive to the status lines to prioritize multiple external devices.

Claim 19 (Previously Presented): The reconfigurable IOC of claim 17, wherein the translation is of a port identified into an SOC address.

Claim 20 (Previously Presented): The reconfigurable IOC of claim 1, wherein the external device includes at least one of a host computer and a central processing unit.

Claim 21 (Previously Presented): The reconfigurable IOC of claim 17, wherein the SOC includes a device chosen from the group comprising an ACE, a storage system, a network access system, and a digital signal processor (DSP).